Amendment to the Specification

Please amend the paragraph beginning on line 1 of page 7 as follows:

Referring to Figs. 3 and 4, a portion of dielectric/insulative well forming layer 30 is removed to form at least one well 34 within well forming layer 30. Such patterning and removal most preferably occurs by photolithography whereby the area outside of well portion 34 is masked with photoresist, and a timed etched is preferably then conducted of layer 30 using a chemistry substantially selective to not remove the photoresist to form the illustrated well 34. Well 34 includes a periphery 35, which peripherally defines an outline of a memory array area and an area 36 peripheral and laterally outward of well 34 which comprises memory peripheral circuitry area. Well 34 also includes a base 38 which, in the preferred illustrated embodiment, is substantially planar. The etch to ~~produce to the~~ produce the illustrated well 34 is preferably timed to provide a lowestmost portion 38 thereof which is received above word line caps 22 by at least 2000 Angstroms. Further, lowestmost portion 38 is preferably received above outermost tops of digit lines 26 by at least 1000 Angstroms and preferably less than 4000 Angstroms. A more preferred distance between base 38 and the outermost tops f the digit lines is from about 2500

Angstroms to about 3500 Angstroms, with 3000 Angstroms being a specific preferred distance.